

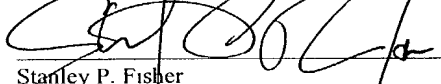
U.S. DEPARTMENT OF COMMERCE PATENT & TRADEMARK OFFICE

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B/O Form PTO 1390		Transmittal Letter to the United States Designated/Elected Office (DO/EO/US) Concerning a Filing Under 35 U.S.C. §371	Attorney's Docket Number NITT.0057
			U.S. Application Number (if known) 10/031377
International Application Number PCT/JP00/05989 ✓	International Filing Date September 4, 2000 ✓	Priority Date Claimed September 9, 1999 ✓	
Title of Invention AN IMAGE DISPLAY AND A DRIVING METHOD OF THE SAME			
Applicant(s) for DO/EO/US Mutsumi SUZUKI, Toshiaki KUSUNOKI, Makoto OKAI, Masakazu SAGAWA and Akitoshi ISHIZAKA			
<p>1. <input checked="" type="checkbox"/> This is a FIRST submission of items concerning a filing under 35 U.S.C. §371.</p> <p>2. <input type="checkbox"/> This is a SECOND or SUBSEQUENT submission of items concerning a filing under 35 U.S.C. §371.</p> <p>3. <input checked="" type="checkbox"/> This is an express request to begin national examination procedures (35 U.S.C. §371(f)). The submission must include items (5), (6), (9) and (21) indicated below.</p> <p>4. <input type="checkbox"/> The US has been elected by the expiration of 19 months from the priority date (Article 31).</p> <p>5. A copy of the International Application as filed (35 U.S.C. §371(c)(2))</p> <p>a. <input type="checkbox"/> is attached hereto (required only if not communicated by the International Bureau).</p> <p>b. <input checked="" type="checkbox"/> has been communicated by the International Bureau.</p> <p>c. <input type="checkbox"/> is not required, as the application was filed in the United States Receiving Office (RO/US).</p> <p>6. A English language translation of the International Application as filed (35 U.S.C. 371(c)(2)).</p> <p>a. <input checked="" type="checkbox"/> is attached hereto.</p> <p>b. <input type="checkbox"/> has been previously submitted under 35 U.S.C. 154(d)(4).</p> <p>7. Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. §371(c)(3))</p> <p>a. <input type="checkbox"/> are attached hereto (required only if not communicated by the International Bureau).</p> <p>b. <input type="checkbox"/> have been communicated by the International Bureau.</p> <p>c. <input type="checkbox"/> have not been made; however, the time limit for making such amendments has NOT expired.</p> <p>d. <input type="checkbox"/> have not been made and will not be made.</p> <p>8. <input type="checkbox"/> An English language translation of the amendments to the claims under PCT Article 19 (35 U.S.C. §371(c)(3)).</p> <p>9. <input checked="" type="checkbox"/> An unexecuted oath or declaration of the inventor(s) (35 U.S.C. 371(c)(4)).</p> <p>10. <input type="checkbox"/> An English language translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. §371(c)(5)).</p> <p>Items 11 to 20 below concern other document(s) or information included:</p> <p>11. <input checked="" type="checkbox"/> An Information Disclosure Statement under 37 C.F.R. §§1.97 and 1.98.</p> <p>12. <input type="checkbox"/> An assignment document for recording. A separate cover sheet in compliance with 37 C.F.R. §§3.28 and 3.31 is included.</p> <p>13. <input type="checkbox"/> A FIRST preliminary amendment.</p> <p>14. <input type="checkbox"/> A SECOND or SUBSEQUENT preliminary amendment.</p> <p>15. <input type="checkbox"/> A substitute specification.</p> <p>16. <input type="checkbox"/> A change of power of attorney and/or address letter.</p> <p>17. <input type="checkbox"/> A computer-readable form of the sequence listing in accordance with PCT Rule 13ter.2 and 35 U.S.C. 1.821-1.825</p> <p>18. <input type="checkbox"/> A second copy of the published international application under 35 U.S.C. 154(d)(4).</p> <p>19. <input type="checkbox"/> A second copy of the English language translation of the international application under 35 U.S.C. 154(d)(4).</p> <p>20. Other items or information:</p>			
Application Number (if known)	International Application Number	Attorney's Docket Number	

10/031377		PCT/JP00/05989	NITT.0057
		CALCULATIONS	PTO USE ONLY
21. <input checked="" type="checkbox"/> The following fees are submitted: Basic National Fee (37 C.F.R. §1.492(a)(1)-(5)): Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2)) paid to USPTO and International Search Report not prepared by the EPO or JPO. 1,040.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but International Search Report prepared by the EPO or JPO. 890.00 International preliminary examination fee (37 CFR 1.482) not paid to USPTO but international search fee (37 CFR 1.445(a)(2)) paid to USPTO. 740.00 International preliminary examination fee (37 CFR 1.482) paid to USPTO but all claims did not satisfy provisions of PCT Article 33(1)-(4) 710.00 International preliminary examination fee (37 CFR 1.482) paid to USPTO and all claims satisfied provisions of PCT Article 33(1)-(4) 100.00			
ENTER APPROPRIATE BASIC FEE AMOUNT		\$890.00	
Surcharge of \$130.00 for furnishing the oath or declaration later than <input type="checkbox"/> 20 <input type="checkbox"/> 30 months from the earliest claimed priority date (37 C.F.R. §1.492(e)).		0.00	
CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE
Total Claims	17	0	x \$18.0
Independent Claims	6	3	x \$84.0
Multiple Dependant Claims (if applicable)		+ 280.00	
TOTAL OF ABOVE CALCULATIONS		1,142.00	
<input type="checkbox"/> Entity claims small entity status. See 37 CFR 1.27. The fees indicated above are reduced by 1/2.		0.00	
SUBTOTAL		1,142.00	
Processing fee of \$130.00 for furnishing the English translation later than 20 30 months from the earliest claimed priority date (37 C.F.R. §1.492(f)).		\$0.00	
TOTAL NATIONAL FEE		1,142.00	
Fee for recording the enclosed assignment (37 C.F.R. § 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 C.F.R. §§ 3.28, 3.31). \$40.00 per property		\$0.00	
TOTAL FEES ENCLOSED		\$ 1,142.00	
		Amount to be Refunded:	\$
		Charged:	\$
a. <input checked="" type="checkbox"/> A check in the amount of \$1,142.00 to cover the national fees is enclosed. b. <input type="checkbox"/> Please charge my Deposit Account Number 08-1480 in the amount of \$ _____ to cover the above fees. A duplicate copy of this sheet is enclosed. c. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Deposit Account Number 08-1480 . A duplicate copy of this sheet is enclosed. d. <input type="checkbox"/> Fees are to be charged to a credit card. WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038. Note.: Where an appropriate time limit under 37 C.F.R. §1 94 or §1 495 has not been met, a petition to revive (37 C.F.R. §1.137(a) or (b)) must be filed and granted to restore the application to pending status.			

Respectfully submitted,



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AN IMAGE DISPLAY AND A DRIVING METHOD OF THE SAME

BACKGROUND OF THE INVENTION

The present invention relates to an image display and a
5 method of driving the same, and particularly to a technology
effective for application to a display apparatus which has
thin-film electron emitters having an
electrode-insulator-electrode structure to emit electrons into
vacuum.

10 The thin-film electron emitters are electron-emitter
elements each using hot electrons produced by applying a high
electric field to an insulator.

As a typical example, an MIM (Metal-Insulator-Metal)
electron emitter comprising a three-layer thin-film structure
15 of a top electrode-insulating layer-base electrode will be
explained.

FIG. 13 is a diagram for describing the principle of
operation of an MIM electron emitter illustrated as a typical
example of a thin-film electron emitter.

20 A driving voltage is applied between a top electrode 11
and a base electrode 13 to set an electric field in a tunneling
insulator 12 to 1 MV/cm to 10MV/cm and over. Thus, electrons
placed in the neighborhood of a Fermi level in the base electrode
13 are transmitted through a barrier by tunneling phenomena.

25 Thereafter they are injected into a conduction band of the

tunneling insulator 12 and further injected into the top electrode 11, thus resulting in hot electrons.

Some of these hot electrons are subjected to scattering under interaction with a solid in the tunneling insulator 12 and the top electrode 11, thus leading to the loss of energy.

As a result, hot electrons having various energies exist when they have reached an interface between the top electrode 11 and vacuum 10.

Of these hot electrons, ones having energy of a work function ϕ or more of the top electrode 11 are emitted into the vacuum 10, and ones other than the above ones flow into the top electrode 11.

Assuming that a current based on the electrons that flows from the base electrode 13 to the top electrode 11, is called a diode current (I_d), and a current based on the electrons emitted into the vacuum 10 is called an emission current (I_e), an electron emission efficiency (I_e/I_d) ranges from about $1/10^3$ to about $1/10^5$.

Incidentally, the MIM thin-film electron emitter has been described in, for example, Japanese Patent Application Laid-Open No. Hei 9-320456.

Now, the top electrode 11 and the base electrode 13 are provided in plural form and these plural top electrodes 11 and base electrodes 13 are made orthogonal to one another to thereby form thin-film electron emitters in matrix form. Consequently,

electron beams can be produced from arbitrary locations and hence they can be used as electron emitters for a display apparatus.

Namely, a display apparatus can be constructed wherein thin-film electron-emitter elements are placed every pixels and electrons emitted therefrom are accelerated in vacuum and thereafter applied to each of phosphors to thereby allow the applied phosphor to emit light, whereby a desired image is displayed thereon.

The thin-film electron emitters have excellent features as electron-emitter elements for the display apparatus in that they are capable of implementing a high-resolution display apparatus because the emitted electron beams are excellent in directionality, and they are easy to handle because they are insusceptible to the influence of their surface contamination, for example.

Even except for the above-described MIM thin-film electron emitter, there are known, as thin-film electron emitters, a MIS (Metal-Insulator-Semiconductor) type (described in, for example, Journal of Vacuum Science and Technologies B, Vol.11, pp. 429 - 432) using a semiconductor as a base electrode, one (described in, for example, Japanese Journal of Applied Physics, Vol. 36, Part 2, No. 7B, pp L939 - L941 (1997)) using a semiconductor-insulator multi-layer film as a tunneling insulator, one (described in, for example, Japanese Journal of Applied Physics, Vol. 34, Part 2, No. 6A, pp. L705 - L707 (1995))

using porous silicon as a tunneling insulator, etc.

A display apparatus using a thin-film electron-emitter matrix makes no use of a shadow mask like a cathode-ray tube (Cathode-ray tube; CRT) and has no beam deflection circuit.

5 Therefore power consumption thereof is slightly lower than that of CRT or the same degree as that.

Power used up or consumed by the thin-film electron-emitter matrix is roughly calculated according to a conventional driving method for the display apparatus using the thin-film
10 electron-emitter matrix.

FIG. 14 is a diagram showing a schematic configuration of a conventional thin-film electron-emitter matrix.

Thin-film electron-emitter elements 301 are respectively formed at points where row electrodes (base electrodes) 310 and
15 column electrodes (top electrodes) 311 intersect respectively.

Incidentally, while the thin-film electron-emitter matrix is illustrated with 3 rows and 3 columns in FIG. 14, the thin-film electron-emitter elements 301 are actually placed by the number of pixels constituting a display apparatus, or the number of
20 sub-pixels in the case of a color display apparatus.

Namely, as the number of rows N and the number of columns M , N ranges from several hundreds of rows to a few thousand rows and M ranges from several hundreds of columns to a few thousand columns as typical examples, respectively.

25 Incidentally, while one pixel is formed of a combination

of respective sub-pixels of red, blue and green in the case of a color image display, ones equivalent to sub-pixels employed in the case of the color image display will be called "pixels" in the present specification. In the present specification, the pixels or sub-pixels are also called "dots".

FIG. 15 is a timing chart for describing the conventional method of driving the display apparatus.

A row electrode driving circuit 41 applies a negative polarity pulse (scan pulse) having amplitude (V_{row}) to one of the row electrodes 310 (a selected scan electrode). Simultaneously column electrode driving circuits 42 apply positive polarity pulses (data pulses) each having amplitude (V_{col}) to some (their corresponding selected column electrodes) of the column electrodes 311.

Since a voltage enough to emit electrons is applied to each thin-film electron-emitter element 301 in which the two pulses overlap each other, the electrons are emitted therefrom. The electrons excite each of phosphors to emit light therefrom.

In the case of the thin-film electron-emitter element 301 free of the application of the positive polarity pulse having the amplitude (V_{col}) thereto, a sufficient voltage is not applied thereto and hence no electron emission is produced.

The row electrodes 310 to be selected, i.e., the row electrodes 310 to which the scan pulse is applied, are successively selected and the data pulses applied to the column

electrodes 311 in association with rows for the selected row electrodes are also changed.

When all the rows are scanned in this way during one field period, an image corresponding to an arbitrary image can be displayed.

During a given period in one field, pulses of reverse polarity (reverse pulses) are respectively applied to all the row electrodes.

Thus, the thin-film electron-emitter elements 301 can be operated stably.

Dissipation power of each driving circuit is calculated according to the conventional driving method when the electrostatic capacitance per one of the thin-film electron-emitter elements 301 is represented as C_e , the number of the column electrodes 311 is represented as M and the number of the row electrodes 310 is represented as N .

The dissipation power is equivalent to power used up or consumed to charge the electrostatic capacitance of each driven element and discharge the same therefrom. The dissipation power does not contribute to light emission.

Dissipation power produced with the application of scan pulses will first be determined.

Dissipation power at the time that a pulse having amplitude (V_{row}), is applied to the corresponding row electrode 310 once, is expressed in the following equation (1):

$$M \cdot C_e \cdot (V_{row})^2 \quad \dots (1)$$

Assuming that the number of refreshing images (field frequency) per second is given as f , the whole dissipation power (P_{row}) for N row electrodes is expressed in the following equation

5 (2):

$$P_{row} = f \cdot N \cdot M \cdot C_e \cdot (V_{row})^2 \quad \dots (2)$$

Similarly, dissipation power (P_r) consumed with the application of reverse pulses is given by the following equation (3):

10
$$P_r = f \cdot N \cdot M \cdot C_e \cdot (V_r)^2 \quad \dots (3)$$

where V_r indicates the voltage amplitude of the reverse pulse applied to the row electrode 310.

Since N thin-film electron-emitter elements 301 are connected to one column electrode 311, the whole dissipation power (P_{col}) for M column electrodes is given by the following equation (4) where pulse voltages are applied to all of the M column electrodes 311:

15

$$P_{col} = f \cdot M \cdot N \cdot (N \cdot C_e \cdot (V_{col})^2) \quad \dots (4)$$

Since the pulses are applied to the column electrodes N times during a screen-refreshing period (one field period), P_{col} is additionally multiplied by N as compared with P_{row} .

20

Incidentally, when pulse voltages are respectively applied to m of the M column electrodes 311, M in the equation (4) is substituted with m .

25 Using $f = 60\text{Hz}$, $N = 480$, $M = 1920$, $C_e = 0.1\text{nF}$, and V_{row}

= $V_r = V_{col} = 4V$ as typical values, for example, results in $P_{row} = P_r = 0.09 [W]$ and $P_{col} = 42 [W]$.

Since, in this case, the power consumption of the thin-film electron-emitter element per se becomes about $1.6 [W]$, the total
5 power consumption results in about $44 [W]$. This is practically problem-free power consumption.

It is however understood that when it is desired to further achieve low power consumption, a reduction in dissipation power P_{col} consumed with the application of the data pulse is effective.

10 Thus, even the prior art presents no problem in terms of power consumption when used as the display apparatus in a similar use as the CRT.

However, the feature of the display apparatus using the thin-film electron emitters is to enable the implementation of
15 a thin flat-panel display.

This type of thin flat-panel display has a use as for a portable display apparatus. In this case, power consumption may preferably be further reduced.

20 SUMMARY .OF THE INVENTION

The present invention has been made to solve the problems of the prior art. An object of the present invention is to provide a technology capable of reducing power consumed by a thin-film electron-emitter matrix in an image display.

25 Another object of the present invention is to provide a

technology capable of reducing power used up or consumed by a thin-film electron-emitter matrix according to a method of driving an image display.

The above, other objects and novel features of the present invention will become apparent from the description of the present specification and the accompanying drawings.

The present invention is characterized in that as shown in a timing chart of FIG. 1, for example, a row electrode 310 placed in a non-selected state are set to a high-impedance state, or row electrodes 310 in a non-selected state and column electrodes 311 in a non-selected state are both set to a high-impedance state.

In order to set the row electrode 310 or column electrode 311 to the high-impedance state, there is known a method of setting an output signal line connected to its corresponding row electrode 310 or column electrode 311 to a floating state inside a row electrode driving circuit 41 or a column electrode driving circuit 42, for example.

Next, power consumption in the thin-film electron-emitter matrix is roughly calculated by the driving method for the image display, according to the present invention.

Let's first consider where the output of the row electrode driving circuit 41 for supplying a driving voltage to the corresponding row electrode 310 held in a non-selected state has been set to a high-impedance state.

FIG. 2 is a diagram showing an equivalent circuit where one row electrode (selected scan line in FIG. 2) 310 is selected and the remaining (N-1) row electrodes (non-selected scan lines in FIG. 2) 310 are respectively brought into a high-impedance state, and simultaneously m column electrodes (selected data lines in FIG. 2) 311 are selected and (M-m) non-selected column electrodes (non-selected data lines in FIG. 2) 311 are respectively fixed to the ground potential.

As shown in FIG. 2, a circuit network extending through the non-selected row electrodes 310 and the non-selected column electrodes 311 must be taken into consideration even in addition to m thin-film electron-emitter elements 301 placed at points where the selected row electrodes 310 and the selected column electrodes 311 intersect respectively.

In the equivalent circuit shown in FIG. 2, electrostatic capacitance $C_1(m)$ between one selected row electrode 310 and the selected column electrodes 311 is expressed in the following equation (5):

$$C_1(m) = \left\{ m + \frac{m(M-m)(N-1)}{M} \right\} C_e \quad \dots (5)$$

FIG. 3 is a graph showing how $C_1(m)$ vary with m.

In FIG. 3, the vertical axis indicates output capacitance of all the column electrodes 311 in units obtained by dividing the same by an electrostatic capacitance per pixel C_e .

In FIG. 3, $N = 500$ and $M = 3000$. In the drawing, marks

O indicate a case based on the conventional driving method and marks ● indicate a case based on the driving method of the present invention.

While $C_1(m)$ reaches the maximum when $m = M/2$, it still becomes 1/4 of the maximum value obtained according to the conventional driving method.

Thus, the driving method of the present invention is capable of reducing dissipation power (P_{col}) consumed with the application of a data pulse to 1/4.

Next consider where each column electrode 311 kept in a non-selected state is also brought into a high-impedance state.

FIG. 4 is a diagram showing an equivalent circuit where one row electrode (selected scan line in FIG. 4) 310 is selected and the remaining $(N-1)$ row electrodes (non-selected scan lines in FIG. 4) 310 are respectively brought into a high-impedance state, and simultaneously m column electrodes (selected data lines in FIG. 4) 311 are selected and $(M-m)$ non-selected column electrodes (non-selected data lines in FIG. 4) 311 are respectively brought into a high-impedance state.

In the equivalent circuit shown in FIG. 4, electrostatic capacitance $C_2(m)$ between one selected row electrode 310 and them selected column electrodes 311 is expressed in the following equation (6):

$$C_2(m) = \left\{ m + \frac{m(M-m)(N-1)}{M+m(N-1)} \right\} C_e \quad \dots (6)$$

FIG. 5 is a graph showing how $C_2(m)$ varies with m .

In FIG. 5, the vertical axis indicates output capacitance of all the column electrodes 311 in units obtained by dividing the output capacitance by electrostatic capacitance per pixel C_e .

In FIG. 5, $N = 500$ and $M = 3000$. In the drawing, marks \circ indicate $C_2(m)$, and marks \bullet indicate a case wherein only non-selected scan electrodes are respectively brought into a high-impedance state for comparison ($C_1(m)$).

When $m = M/2$, for example, $C_2(m)$ is further reduced to 1/100 or less as compared with $C_1(m)$.

Thus, the driving method of the present invention is capable of reducing the dissipation power (P_{co1}) incident to the application of the data pulse to 1/100 or less as compared with the conventional one.

In general, a driving method of a matrix-addressed display such as a liquid-crystal display or the like avoids the setting of a given electrode to a high-impedance state.

This is because when there is an electrode held in a high-impedance state, a crosstalk phenomenon is apt to occur, and hence degradation in image quality occurs and failures such as the inability to display a desired image in some cases occur.

The present inventors have focused attention on the fact that the crosstalk due to the introduction of such a high-impedance state will occur because the voltage of the

electrode held in the high-impedance state is not fixed, depending on the number of lighting dots (i.e., displayed image) in its peripheral dots, and/or the voltage of its adjacent electrode, etc.

5 Another point that has led to the devisal of the present invention, resides in that the present inventors have focused attention on the fact that a thin-film electron emitter does not emit electrons unless a sufficient current is supplied thereto from an external circuitry, i.e., it has an aspect that
10 will operate as a current-driven device.

As mentioned previously, the mechanism of emitting the electrons from each thin-film electron emitter uses the tunneling current generated by the electric field lying within the tunneling insulator as the hot electrons, and therefore is of
15 a voltage-driven type in this respect.

Since, however, the emission current (I_e) is about 10^{-3} of the tunneling current, a current of about 10^3 times the emission current must be supplied from an external circuitry to obtain a desired emission current. Therefore, the electron emission
20 mechanism has an aspect that operates as a current-driven device.

Therefore, the thin-film electron emitter does not cause electron emission if the impedance thereof is sufficiently high even if the potential at each electrode is other than a desired value.

25 Therefore, the thin-film electron emitter does not cause

the crosstalk even if the driving method of the present invention is used.

The present invention has been made on the basis of the above findings. A summary of a typical one of the inventions disclosed in the present application will be described in brief
5 as follows:

There is provided an image display which comprises a display device including a first plate which has a plurality of electron-emitter elements each having a structure comprised of
10 a base electrode, an insulating layer and a top electrode stacked on one another in this order, the electron-emitter element emitting electrons from the surface of the top electrode when a voltage of positive polarity is applied to the top electrode; a plurality of first electrodes for respectively applying driving
15 voltages to the base electrodes of the electron-emitter elements lying in a row (or column) direction, of the plurality of electron-emitter elements; and a plurality of second electrodes for respectively applying driving voltages to the top electrodes of the electron-emitter elements lying in the column (or row)
20 direction, of the plurality of electron-emitter elements, a frame component, and a second plate having phosphors, whereby a space surrounded by the first plate, the frame component and the second plate is brought to vacuum, wherein the first electrode held in the non-selected state is set to a state of having an impedance
25 higher than that of the corresponding first electrode held in

the selected state, or each of the first and second electrodes held in the non-selected state is set to a state of having an impedance higher than that of each of the first and second electrodes held in the selected state.

5 Incidentally, a prior-art search has been carried out based on the result of the present invention from the viewpoint that each electrode held in the non-selected state is brought into high impedance.

10 As a result, the corresponding art has not been found in the display apparatus using the thin-film electron emitters, which is intended for the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

15 FIG. 1 is a diagram for describing a method of driving an image display of the present invention;

 FIG. 2 is a diagram showing an equivalent circuit for calculating the capacitance between electrodes according to the method of driving the image display of the present invention;

20 FIG. 3 is a graph showing changes in the capacitance between the electrodes calculated by the equivalent circuit shown in FIG. 2;

 FIG. 4 is a diagram illustrating an equivalent circuit for calculating the capacitance between electrodes according to the method of driving the image display of the present
25 invention;

FIG. 5 is a graph showing changes in the capacitance between the electrodes calculated by the equivalent circuit shown in FIG. 4;

FIG. 6 is a plan view illustrating a configuration of part
5 of a thin-film electron-emitter matrix of a cathode plate employed in an embodiment 1 of the present invention;

FIG. 7 is a plan view showing the relationship in position between the cathode plate and a phosphor plate employed in the embodiment 1 of the present invention;

10 FIGS. 8(a) and 8(b) are respectively fragmentary cross-sectional views depicting a configuration of a display apparatus according to the embodiment 1 of the present invention;

FIGS. 9(a) through 9(f) are respectively diagrams for describing a method of manufacturing a cathode plate employed
15 in the embodiment 1 of the present invention;

FIG. 10 is a connection diagram illustrating a state in which driving circuits are connected to a display panel employed in the embodiment 1 of the present invention;

FIG. 11 is a timing chart showing one example illustrative
20 of waveforms of driving voltages outputted from the respective driving circuits shown in FIG. 10;

FIG. 12 is a timing chart showing one example illustrative of waveforms of driving voltages outputted from row electrode and column electrode driving circuits in an image display
25 according to an embodiment 2 of the present invention;

FIG. 13 is a diagram for describing the principle of operation of a thin-film electron emitter;

FIG. 14 is a diagram showing a schematic configuration of a conventional thin-film electron-emitter matrix; and

5 FIG. 15 is a diagram for describing a conventional method of driving a display apparatus.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Preferred embodiments of the present invention will
10 hereinafter be described in detail with reference to the accompanying drawings.

Incidentally, elements of structure each having the same function in all drawings for describing the embodiments are respectively identified by the same reference numerals and their
15 repetitive description will therefore be omitted.

[Embodiment 1]

An image display according to an embodiment 1 of the present invention has a configuration wherein a display panel (display device of the present invention) in which brightness-modulation
20 elements for respective dots are formed according to combinations of a thin-film electron-emitter matrix corresponding to an electron emitter used for emitting electrons and phosphors, is used to connect driving circuits to row electrodes and column electrodes of the display panel respectively.

25 Now the display panel comprises a cathode plate formed

with a thin-film electron-emitter matrix, and a phosphor plate formed with phosphor patterns.

FIG. 6 is a plan view showing a configuration of part of a thin-film electron-emitter matrix of a cathode plate according to the present embodiment, and FIG. 7 is a plan view showing the relationship in position between the cathode plate and phosphor plate according to the present embodiment, respectively.

FIG. 8 is a fragmentary cross-sectional view showing a configuration of the display apparatus according to the present embodiment, wherein FIG. 8(a) is cross-sectional views taken along cut lines A - B shown in FIGs. 6 and 7, and FIG. 8(b) is cross-sectional views taken along cut lines C - D shown in FIGs. 6 and 7.

However, the illustration of a plate 14 is omitted from FIGs. 6 and 7.

Further, a reduction scale as viewed in a vertical height direction is arbitrary in FIG. 8. Namely, while base electrodes 13, top electrode buslines 32, and the like are respectively less than or equal to a few μm in thickness, the distance between the plate 14 and a plate 110 is equivalent to a length of from about 1mm to about 3mm.

While the following description is made using an electron-emitter matrix with 3 rows and 3 columns, it is needless to say that the numbers of rows and columns in an actual display

panel respectively result in several hundreds rows to a few thousand rows, and a few thousand columns.

In FIG. 6, regions 35 surrounded by dot lines indicate electron-emission regions (electron-emitter elements in the present invention) respectively.

Each of the electron-emission regions 35 emits electrons into vacuum from within its area or region at a location defined by a tunneling insulator 12.

Since the electron-emission region 35 is not represented on a plan view because it is covered with a top electrode 11, it is illustrated by a dotted line.

FIG. 9 is a diagram for describing a method of manufacturing a cathode plate employed in the present embodiment.

A method of fabricating a thin-film electron-emitter matrix of the cathode plate employed in the present embodiment will be explained below with reference to FIG. 9.

Incidentally, while only one thin-film electron emitter 301 formed at the intersection of one of row electrodes 310 and one of column electrodes 311 (both shown in FIGs. 6 and 7), is extracted and plotted in FIG. 9, a plurality of thin-film electron emitters 301 are actually arranged in matrix form as illustrated in FIGs. 6 and 7.

Further, the right columns shown in FIG. 9 are respectively plan views, whereas the left columns are respectively cross-sectional views taken along lines A - B in the views on

the right side.

An electrically conductive film for a base electrode 13 is formed with a thickness of 300nm, for example, on an insulative substrate 14 such as glass or the like.

5 As a material for the base electrode 13, may be used, for example, an aluminum (Al: hereinafter called "Al") alloy.

In the present method, an Al-neodymium (Nd: hereinafter called "Nd") alloy is used.

10 For example, a sputtering method, resistive-heating evaporation or the like may be used to form such an Al alloy film.

Next, the Al alloy film is processed into strip form by resist formation using photolithography and etching following it to thereby form a base electrode 13 as shown in FIG. 9(a).

15 The base electrode 13 assumes the role of the row electrode 310.

A resist used herein may be one suitable for etching, and both of wet etching and dry etching may be used as the etching.

20 Next, a resist is applied and exposed with an ultraviolet-ray, followed by patterning, thereby forming a resist pattern 501 as shown in FIG. 9(b).

As the resist, may be used, for example, a quinonediazide positive resist.

25 Next, anodic oxidation is done while the resist pattern 501 remains attached to the base electrode 13 to thereby form

a protection layer 15 as shown in FIG. 9(c).

In the present embodiment, an anodization voltage was set to about 100V upon such anodic oxidation, and the thickness of the protection layer 15 was set to about 140nm.

5 The resist pattern 501 is removed with an organic solvent such as acetone or the like and thereafter the surface of the base electrode 13 covered with the resist is anodically oxidized again to thereby form a tunneling insulator 12 as shown in FIG. 9(d).

10 In the present embodiment, an anodization voltage was set to 6V upon such re-anodization, and the thickness of the tunneling insulator was set to 8nm.

 Next, an electrically conductive film for a top electrode busline 32 is formed and the resist is patterned and subjected
15 to etching to thereby form the top electrode busline 32 as shown in FIG. 9(e).

 In the present embodiment, the top electrode busline 32 made use of the Al alloy, and the thickness thereof was set to about 300nm.

20 Incidentally, gold (Au) or the like may be used as a material for the top electrode busline 32.

 Incidentally, the top electrode busline 32 is provided in such a way that the edges of the pattern therefor are etched so as to take a taper-shape and a top electrode 11 to be formed
25 subsequently will not cause a break due to a step at the edges

of the pattern.

Here, the top electrode busline 32 shares the role of the column electrode 311.

5 Next, an iridium (Ir) having a thickness of 1nm, a platinum (Pt) having a thickness of 2nm, and a gold (Au) having a thickness of 3nm are formed by sputtering in that order.

According to a resist and patterning by etching, a multi-layer film of Ir-Pt-Au is patterned as the top electrode 11 as shown in FIG. 9(f).

10 Incidentally, a region 35 surrounded by a dotted line indicates an electron emission region in FIG. 9(f).

The electron-emission region 35 emits electrons into vacuum from within its area or region at a location defined by the tunneling insulator 12.

15 The thin-film electron-emitter matrix is completed on the plate 14 according to the above-described process.

In the thin-film electron-emitter matrix as described above, electrons are emitted from the region (electron-emission region 35) defined by the tunneling insulator 12, i.e., the region
20 defined by the resist pattern 501.

Further, since the protection layer 15, which is of a thick insulating film, is formed around the perimeter of the electron-emission region 35, an electric field applied between the top electrode and the base electrode does not concentrate
25 at sides or edges of the base electrode 13 and hence an electron

emission characteristic stable over a long time is obtained.

The phosphor plate according to the present embodiment comprises black matrixes 120 formed on a plate 110 such as sodalime glass or the like, phosphors (114A through 114C) of red (R), green (G) and blue (B), which are formed within trenches or grooves of the black matrixes 120, and a metal back film 122 formed over these.

A method of manufacturing the phosphor plate according to the present embodiment will be explained below.

The black matrixes 120 are formed on the plate 110 with the object of increasing the contrast ratio of the display apparatus (see FIG. 8(b)).

Next, the red phosphor 114A, green phosphor 114B and blue phosphor 114C are formed.

These phosphors were patterned by photolithography in a manner similar to being used in the phosphor screen of the normal cathode-ray tube.

As the phosphors, for example, $Y_2O_2S : Eu$ (P22-R), $ZnS : Cu, Al$ (P22-G), and $ZnS : Ag$ (P22-B) were respectively used as red, green and blue.

Next, filming is effected on the plate 110 with a film such as nitrocellulose or the like and thereafter Al is evaporated onto the entire plate 110 with a thickness of from about 50nm to about 300nm to thereby produce the metal back film 122.

Thereafter, the plate 110 is heated at about 400°C to

pyrolize organic substances such as a filming film, PVA, etc.
The phosphor plate is completed in this way.

The cathode plate and phosphor plate fabricated in this
way are sealed with frit glass with a spacer 60 interposed
5 therebetween.

A relationship of positions between the phosphors (114A
through 114C) formed in the phosphor plate and the thin-film
electron-emitter matrix of the cathode plate is represented as
shown in FIG. 7.

10 Incidentally, the components on the plate 110 are
illustrated only by oblique lines alone in FIG. 7 to show the
relationship of positions between the phosphors (114A through
114C), the black matrixes 120 and the components.

The relationship between the electron-emission region 35,
15 i.e., the portion where the tunneling insulator 12 is formed,
and the width of each phosphor 114 is of importance.

In the present embodiment, the width of the
electron-emission region 35 is designed so as to be narrower
than that of each of the phosphors (114A through 114C) in
20 consideration of an electron beam emitted from the thin-film
electron emitter 301 being slightly broadened spatially.

Further, the distance between the plate 110 and the plate
14 was set so as to range from about 1mm to about 3mm.

The spacer 60 is inserted to prevent breakage of the display
25 panel due to an external force of atmospheric pressure when the

interior of the display panel is vacuumized.

Thus, when a display apparatus having a display area represented by less than or equal to a width of about 4cm x a length of about 9cm is fabricated by using glass having a thickness of 3mm as for the plates 14 and 110, it can endure the atmospheric pressure owing to mechanical strengths of the plates 110 and 14 per se. It is therefore unnecessary to insert the spacer 60.

The spacer 60 is shaped in the form of a rectangular parallelepiped as shown in FIG. 7 by way of example.

While there are provided posts for the spacers 60 every three rows in the present embodiment, the number of the posts (layout density) may be reduced within an endurable range of mechanical strength.

Plate-shaped or cylindrical or pillar-shape posts made up of glass or ceramic are placed as the spacers 60.

Incidentally, while the spacer 60 seems like being not in contact with the plate 14 in FIG. 8(a), it is actually in contact with the column electrodes 311 on the plate 14.

In FIG. 8(a), a clearance can be defined by the thickness of the column electrode 311.

The sealed display panel is sealed off by being pumped to a vacuum of about 1×10^{-7} Torr.

In order to maintain the degree of vacuum in the display panel in a high vacuum, a getter film is formed or a getter material

is activated at a predetermined position (not shown) lying within the display panel immediately before or after its sealing.

In the case of a getter material with barium (Ba) as a principal component, a getter film can be formed by inductive heating.

The display panel using the thin-film electron-emitter matrix is completed in this way.

Since the distance between the plate 110 and the plate 14 extends long so as to range from about 1mm to about 3mm in the present embodiment, an acceleration voltage applied to the metal back 122 can be set to a high voltage of 3KV to 6KV. Thus the phosphors for the cathode-ray tube (CRT) can be used for the phosphors (114A through 114C) as described above.

FIG. 10 is a connection diagram showing a state in which driving circuits are connected to the display panel according to the present embodiment.

Row electrodes 310 (base electrodes 13) are respectively connected to row electrode driving circuits 41, and column electrodes 311 (top electrode buslines 32) are respectively connected to column electrode driving circuits 42.

Connections between the respective driving circuits (41 and 42) and a cathode plate are made by, for example, one obtained by subjecting a tape carrier package to connect-by-pressure by means of an anisotropically conductive film, or chip-on-glass or the like obtained by directly implementing a semiconductor

chip constituting each of the driving circuits (41 and 42) on the plate 14 of the cathode plate.

An acceleration voltage, which ranges from about 3KV to about 6KV, is always applied to the metal back film 122 from an acceleration voltage source 43.

FIG. 11 is a timing chart showing one example illustrative of waveforms of driving voltages outputted from the respective driving circuits shown in FIG. 10.

Incidentally, dotted lines indicate high-impedance outputs respectively in the same drawings.

In fact, the output impedance may be set so as to range from about $1\text{M}\Omega$ to about $10\text{M}\Omega$. In the present embodiment, it was set to $5\text{M}\Omega$.

Let's now assume that an nth row electrode 310 is represented as R_n , an mth column electrode 311 is represented as C_m , and a dot for an intersection of the nth row electrode 310 and the mth column electrode 311 is represented as (n, m) .

At a time t_0 , any electrode carries a voltage of 0 and hence no electrons are emitted, whereby the phosphors (114A through 114C) do not emit light.

At a time t_1 , the row electrode driving circuit 41 applies a driving voltage of (V_{R1}) to its corresponding row electrode 310 of R_1 , and the column electrode driving circuits 42 apply a driving voltage of (V_{C1}) to their corresponding column electrodes 311 of $(C_1$ and $C_2)$.

Since a voltage of $(V_{C1} - V_{R1})$ is applied between the top electrode 11 and the base electrode 13 for dots (1, 1) and (1, 2), thin-film electron emitters for the two dots emit electrons into vacuum if the voltage of $(V_{C1} - V_{R1})$ is set to greater than or equal to a threshold voltage for electron emission.

In the present embodiment, $V_{R1} = -5V$ and $V_{C1} = 4.5V$.

The emitted electrons are accelerated under the voltage applied to the metal back film 122 and thereafter collide with the phosphors (114A through 114C) to thereby allow the phosphors (114A through 114C) to emit light.

Since the row electrodes 310 of others (R2 and R3) are respectively held in a high-impedance state during this period, no electrons are emitted regardless of the voltage values of the column electrodes 311, and hence the corresponding phosphors (114A through 114C) do not emit light either.

When the row electrode driving circuit 41 applies the driving voltage of (V_{R1}) to its corresponding row electrode 310 of R2, and the column electrode driving circuit 42 applies the voltage of (V_{C1}) to its corresponding column electrode 311 of C1 at a time $t2$, a dot (2, 1) lights up similarly.

When the driving voltages having such voltage waveforms as shown in FIG. 11 are applied to their corresponding row and column electrodes 310 and 311, only dots diagonally shaded in FIG. 10 light up.

In this way, changing the signals applied to the column

electrodes 311 allows the display of a desired image or information.

By suitably changing the magnitude of the driving voltage (V_{C1}) applied to each column electrode 311 in accordance with
5 an image signal, an image having a gray scale can be displayed.

Incidentally, in order to release the charges accumulated in the tunneling insulator 12, the row electrode driving circuits 41 apply a driving voltage of (V_{R2}) to all of the row electrodes 310 and simultaneously the column electrode driving circuits
10 42 apply a driving voltage of 0V to all of the column electrodes at a time $t4$ in FIG. 11.

Since $V_{R2} = 5V$ now, a voltage of a $-V_{R2} = -5V$ is applied to each thin-film electron emitter 301.

Applying the voltage (reverse pulse) of polarity opposite
15 to upon electron emission in this way allows an improvement in lifetime characteristic of each thin-film electron emitter.

Incidentally, the use of a vertical blanking period of a video signal as reverse pulse applying periods (see $t4$ to $t5$ and $t8$ to $t9$ in FIG. 11) yields satisfactory matching with the
20 video signal.

Since the row electrodes 310 each held in the non-selected state are set to the high-impedance state in the present embodiment as described above, power consumption can be reduced as mentioned previously.

25 [Embodiment 2]

A display panel employed in an image display according to an embodiment 2 of the present invention, and a method of connecting the display panel and driving circuits are identical to those in the aforementioned embodiment.

5 FIG. 12 is a timing chart showing one example illustrative of waveforms of driving voltages outputted from row electrode driving circuits 41 and column electrode driving circuits 42 employed in the image display according to the embodiment 2 of the present invention.

10 Incidentally, an acceleration voltage source 43 always applies an acceleration voltage of about 3KV to about 6KV to a metal back film 122 even in the case of the present embodiment.

In FIG. 12, dotted lines indicate high-impedance outputs respectively.

15 In fact, the output impedance may be set so as to range from about $1\text{M}\Omega$ to about $10\text{M}\Omega$. In the present embodiment, it was set to $5\text{M}\Omega$.

20 Let's now assume that in a manner similar to the embodiment 1, an nth row electrode 310 is represented as R_n , an mth column electrode 311 is represented as C_m , and a dot for an intersection of the nth row electrode 310 and the mth column electrode 311 is represented as (n, m) .

25 At a time t_0 , any electrode carries a voltage of 0 and hence no electrons are emitted, whereby phosphors (114A through 114C) do not emit light.

At a time t_1 , the row electrode driving circuit 41 applies a driving voltage of (V_{R1}) to its corresponding row electrode 310 of R1, and the column electrode driving circuits 42 apply a driving voltage of (V_{C1}) to their corresponding column electrodes 311 of (C1 and C2).

Since a voltage of $(V_{C1} - V_{R1})$ is applied between a top electrode 11 and a base electrode 13 for dots (1, 1) and (1, 2), thin-film electron emitters for the two dots emit electrons into vacuum if the voltage of $(V_{C1} - V_{R1})$ is set to greater than or equal to a threshold voltage for electron emission.

In the present embodiment, $V_{R1} = -5V$ and $V_{C1} = 4.5V$.

The emitted electrons are accelerated under the voltage applied to the metal back film 112 and thereafter collide with the phosphors (114A through 114C) to thereby allow the phosphors (114A through 114C) to emit light.

Since the row electrodes 310 of others (R2 and R3) are respectively held in a high-impedance state during this period, no electrons are emitted regardless of the voltage values of the column electrodes 311, and hence the corresponding phosphors (114A through 114C) do not emit light either.

Since the column electrode 311 of C3 is held in the high-impedance state during this period, no electrons are emitted from a dot (1, 3) and hence the corresponding phosphors (114A through 114C) do not emit light either.

When the row electrode driving circuit 41 applies the

driving voltage of (V_{R1}) to its corresponding row electrode 310 of R2, and the column electrode driving circuit 42 applies the voltage of (V_{C1}) to its corresponding column electrode 311 of C1 at a time t_2 , a dot (2, 1) lights up similarly.

5 When the driving voltages having such voltage waveforms as shown in FIG. 12 are now applied to their corresponding row and column electrodes 310 and 311, only dots diagonally shaded in FIG. 10 light up.

10 In this way, changing the signals applied to the column electrodes 311 allows the display of a desired image or information.

By suitably changing a pulse width of the driving voltage (V_{C1}) applied to each column electrode 311 in accordance with an image signal, an image having a gray scale can be displayed.

15 In order to release the charges accumulated in a tunneling insulator 12, the row electrode driving circuits 41 apply a driving voltage of (V_{R2}) to all of the row electrodes 310 and simultaneously the column electrode driving circuits 42 apply a driving voltage of 0V to all of the column electrodes at a
20 time t_4 in FIG. 12.

Since $V_{R2} = 5V$ now, a voltage of a $-V_{R2} = -5V$ is applied to each thin-film electron emitter 301.

Applying the voltage (reverse pulse) of polarity opposite to upon electron emission in this way allows an improvement in
25 lifetime characteristic of each thin-film electron emitter.

Incidentally, the use of a vertical blanking period of a video signal as reverse pulse applying periods (see t4 to t5 and t8 to t9 in FIG. 12) yields satisfactory matching with the video signal.

5 Since the column electrodes 311 each held in a non-selected state are also set to the high-impedance state as well as the row electrodes 310 each held in a non-selected state in the present embodiment as described above, power consumption can further be reduced as compared with the embodiment 1 as mentioned
10 previously.

 While the invention made by the present inventors has been described specifically by the illustrated embodiments, the present invention is not limited to the embodiments. It is needless to say that various changes can be made thereto within
15 the scope not departing from the substance thereof.

 An image display and a driving method thereof according to the present invention, particularly, a display apparatus using thin-film electron emitters for respectively emitting electrons into vacuum is intended for the implementation of a technology
20 capable of reducing dissipation power incident to the driving of a thin-film electron emitter array and thereby reducing power consumption. This can provide great industrial applicability.

WHAT IS CLAIMED IS:

1. An image display comprising:

a display device including,

a first plate having,

5 a plurality of electron-emitter elements each having a structure comprised of a base electrode, an insulating layer and a top electrode stacked on one another in this order, said electron-emitter element emitting electrons from the surface of the top electrode when a voltage of positive polarity is applied
10 to the top electrode;

a plurality of first electrodes for respectively applying driving voltages to the base electrodes of the electron-emitter elements lying in a row (or column) direction, of said plurality of electron-emitter elements; and

15 a plurality of second electrodes for respectively applying driving voltages to the top electrodes of the electron-emitter elements lying in the column (or row) direction, of said plurality of electron-emitter elements;

a frame component; and

20 a second plate having phosphors;

wherein a space surrounded by said first plate, said frame component and said second plate is brought into vacuum;

first driving means for supplying driving voltages to said respective first electrodes; and

25 second driving means for supplying driving voltages to

said respective second electrodes;

wherein said first driving means sets the first electrode held in a non-selected state to a state of having an impedance higher than that of the first electrode held in a selected state.

5

2. An image display comprising:

a display device including,

a first plate having,

10 a plurality of electron-emitter elements each having a structure comprised of a base electrode, an insulating layer and a top electrode stacked on one another in this order, said electron-emitter element emitting electrons from the surface of the top electrode when a voltage of positive polarity is applied to the top electrode;

15 a plurality of first electrodes for respectively applying driving voltages to the base electrodes of the electron-emitter elements lying in a row (or column) direction, of said plurality of electron-emitter elements; and

20 a plurality of second electrodes for respectively applying driving voltages to the top electrodes of the electron-emitter elements lying in the column (or row) direction, of said plurality of electron-emitter elements;

a frame component; and

a second plate having phosphors;

25 wherein a space surrounded by said first plate, said frame

component and said second plate is brought into vacuum;

first driving means for supplying driving voltages to said
respective first electrodes; and

second driving means for supplying driving voltages to
5 said respective second electrodes;

wherein said first driving means sets the first electrode
held in a non-selected state to a state of having an impedance
higher than that of the first electrode held in a selected state,
and

10 wherein said second driving means sets the second electrode
held in a non-selected state to a state of having an impedance
higher than that of the second electrode held in a selected state.

3. An image display according to claim 1, wherein said
15 high impedance is an impedance of $1M\Omega$ or more.

4. An image display according to claim 1, wherein said
first driving means brings a first electrode held in a
non-selected state to a floating state.

20

5. An image display according to claim 2, wherein said
second driving means brings a second electrode held in a
non-selected state to a floating state.

25

6. An image display according to claim 1, wherein said

each electron-emitter element includes a top electrode busline which is electrically connected to the top electrode and functions as the second electrode.

5 7. An image display according to claim 1, wherein said first electrode functions as the base electrode of said each electron-emitter element.

10 8. An image display according to claim 1, wherein said base electrode comprises a metal.

 9. An image display according to claim 1, wherein said base electrode comprises a semiconductor.

15 10. An image display according to claim 1, wherein said insulating layer comprises a multi-layer film of a semiconductor and an insulator.

20 11. A driving method of an image display comprising,
a first plate having,
a plurality of electron-emitter elements each having a structure comprised of a base electrode, an insulating layer and a top electrode stacked on one another in this order, said electron-emitter element emitting electrons from the surface
25 of the top electrode when a voltage of positive polarity is applied

to the top electrode;

a plurality of first electrodes for respectively applying driving voltages to the base electrodes of the electron-emitter elements lying in a row (or column) direction, of said plurality
5 of electron-emitter elements; and

a plurality of second electrodes for respectively applying driving voltages to the top electrodes of the electron-emitter elements lying in the column (or row) direction, of said plurality of electron-emitter elements;

10 a frame component; and

a second plate having phosphors;

wherein a space surrounded by said first plate, said frame component and said second plate is brought into vacuum, said method comprising the step of:

15 setting the first electrode held in a non-selected state to a state of having an impedance higher than that of the first electrode held in a selected state.

12. A driving method of an image display comprising,

20 a first plate having,

a plurality of electron-emitter elements each having a structure comprised of a base electrode, an insulating layer and a top electrode stacked on one another in this order, said electron-emitter element emitting electrons from the surface
25 of the top electrode when a voltage of positive polarity is applied

to the top electrode;

a plurality of first electrodes for respectively applying driving voltages to the base electrodes of the electron-emitter elements lying in a row (or column) direction, of said plurality
5 of electron-emitter elements; and

a plurality of second electrodes for respectively applying driving voltages to the top electrodes of the electron-emitter elements lying in the column (or row) direction, of said plurality of electron-emitter elements;

10 a frame component; and

a second plate having phosphors;

wherein a space surrounded by said first plate, said frame component and said second plate is brought into vacuum, said method comprising the steps of:

15 setting the first electrode held in a non-selected state to a state of having an impedance higher than that of the first electrode held in a selected state; and

setting the second electrode held in a non-selected state to a state of having an impedance higher than that of the second
20 electrode held in a selected state.

13. A driving method according to claim 11, wherein said high impedance is an impedance of $1M\Omega$ or more.

25 14. A driving method according to claim 11, further

including the step of bringing the first electrode held in the non-selected state to a floating state.

15. A driving method according to claim 12, further
5 including the step of bringing the second electrode held in the non-selected state to a floating state.

16. An image display comprising:
a display device including,
10 a first plate having,
a plurality of thin-film electron emitters each having a base electrode and a top electrode, said each thin-film electron emitter emitting electrons from the surface of the top electrode when a voltage of positive polarity is applied to the top
15 electrode;

a plurality of first electrodes for respectively applying driving voltages to the base electrodes of the thin-film electron emitters lying in a row (or column) direction, of said plurality of thin-film electron emitters; and

20 a plurality of second electrodes for respectively applying driving voltages to the top electrodes of the thin-film electron emitters lying in the column (or row) direction, of said plurality of thin-film electron emitters;

a frame component; and
25 a second plate having phosphors;

wherein a space surrounded by said first plate, said frame component and said second plate is brought into vacuum;

first driving means for supplying driving voltages to said respective first electrodes; and

5 second driving means for supplying driving voltages to said respective second electrodes;

wherein said first driving means sets the first electrode held in a non-selected state to a state of having an impedance higher than that of the first electrode held in a selected state.

10

17. An image display comprising:

a display device including,

a first plate having,

15 a plurality of thin-film electron emitters each having a base electrode and a top electrode, said each thin-film electron emitter emitting electrons from the surface of the top electrode when a voltage of positive polarity is applied to the top electrode;

20 a plurality of first electrodes for respectively applying driving voltages to the base electrodes of the thin-film electron emitters lying in a row (or column) direction, of said plurality of thin-film electron emitters; and

25 a plurality of second electrodes for respectively applying driving voltages to the top electrodes of the thin-film electron emitters lying in the column (or row) direction, of said plurality

of thin-film electron emitters;

a frame component; and

a second plate having phosphors;

wherein a space surrounded by said first plate, said frame
5 component and said second plate is brought into vacuum;

first driving means for supplying driving voltages to said
respective first electrodes; and

second driving means for supplying driving voltages to
said respective second electrodes;

10 wherein said first driving means sets the first electrode
held in a non-selected state to a state of having an impedance
higher than that of the first electrode held in a selected state,
and

wherein said second driving means sets the second electrode
15 held in a non-selected state to a state of having an impedance
higher than that of the second electrode held in a selected state.

ABSTRACT OF THE DISCLOSURE

The present invention provides an image display capable of reducing power used up or consumed by a thin-film

5 electron-emitter matrix. As a typical one, there is provided an image display which comprises a display device including a first plate which has a plurality of electron-emitter elements each having a structure comprised of a base electrode, an insulating layer and a top electrode stacked on one another in
10 this order, the electron-emitter element emitting electrons from the surface of the top electrode when a voltage of positive polarity is applied to the top electrode; a plurality of first electrodes for respectively applying driving voltages to the base electrodes of the electron-emitter elements lying in a row
15 direction, of the plurality of electron-emitter elements; and a plurality of second electrodes for respectively applying driving voltages to the top electrodes of the electron-emitter elements lying in a column direction, of the plurality of electron-emitter elements, a frame component, and a second plate
20 having phosphors, wherein a space surrounded by the first plate, the frame component and the second plate is brought into vacuum. In the image display, the first electrode and/or the second electrode held in a non-selected state is set to a high-impedance state.

FIG. 1

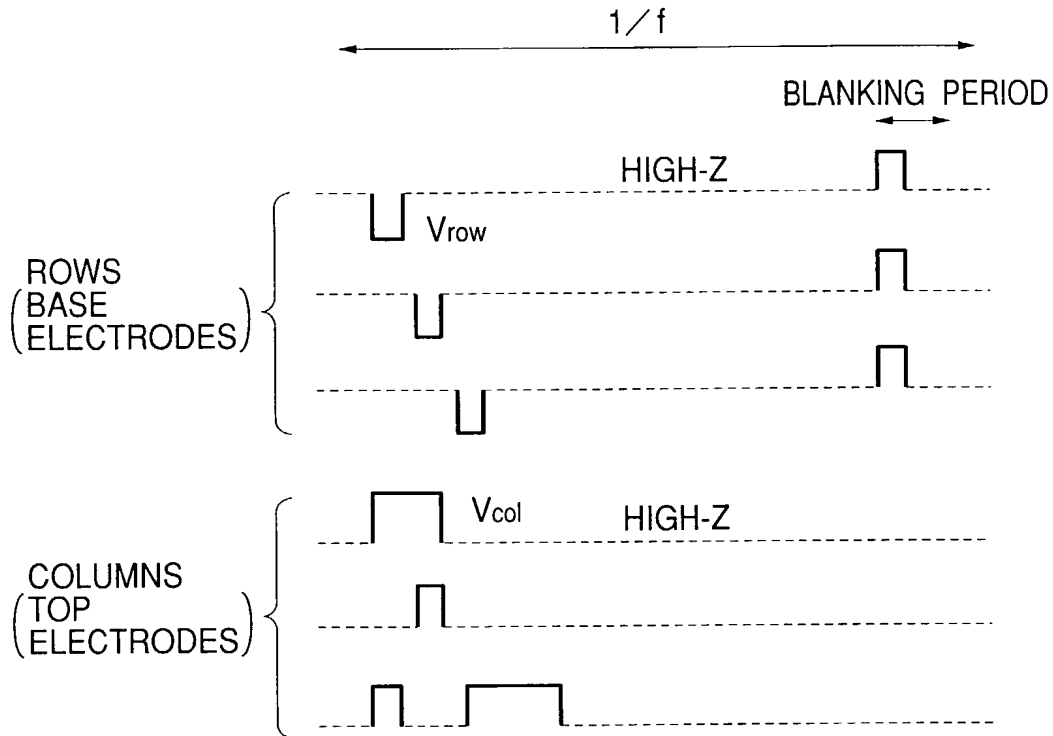


FIG. 2

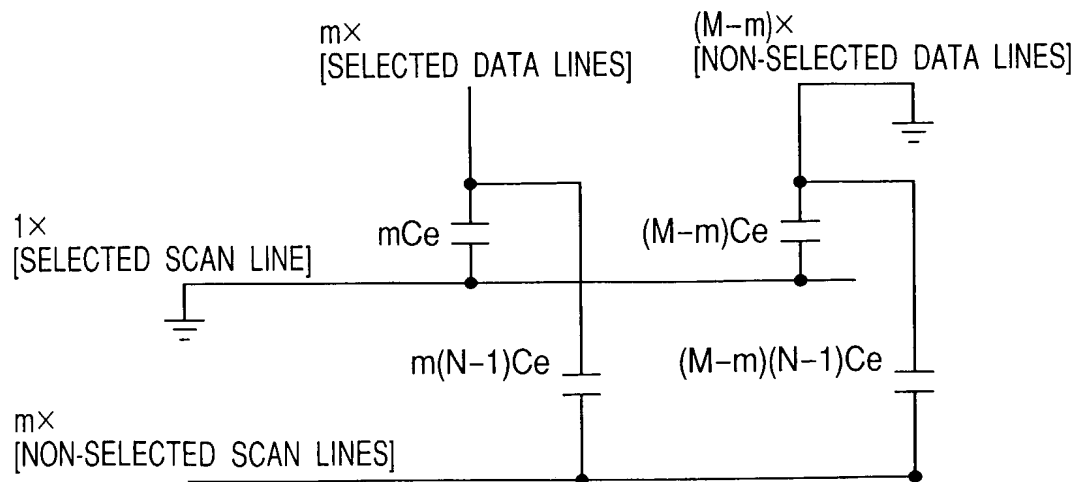


FIG. 3

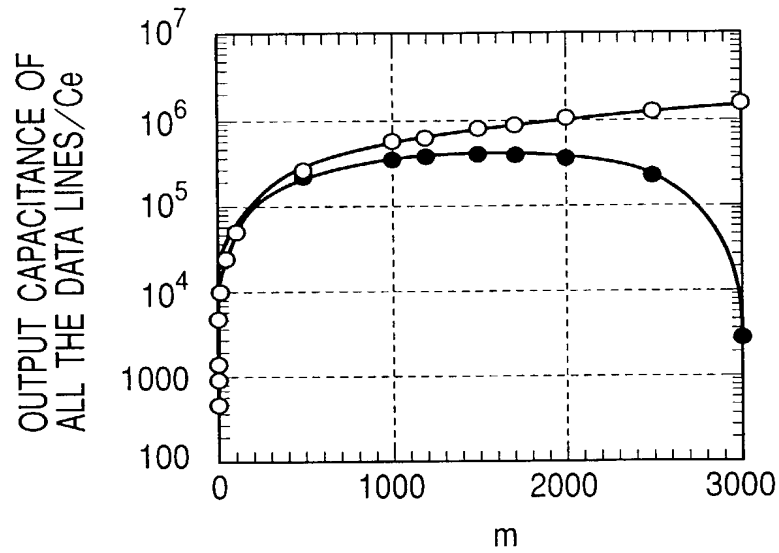


FIG. 4

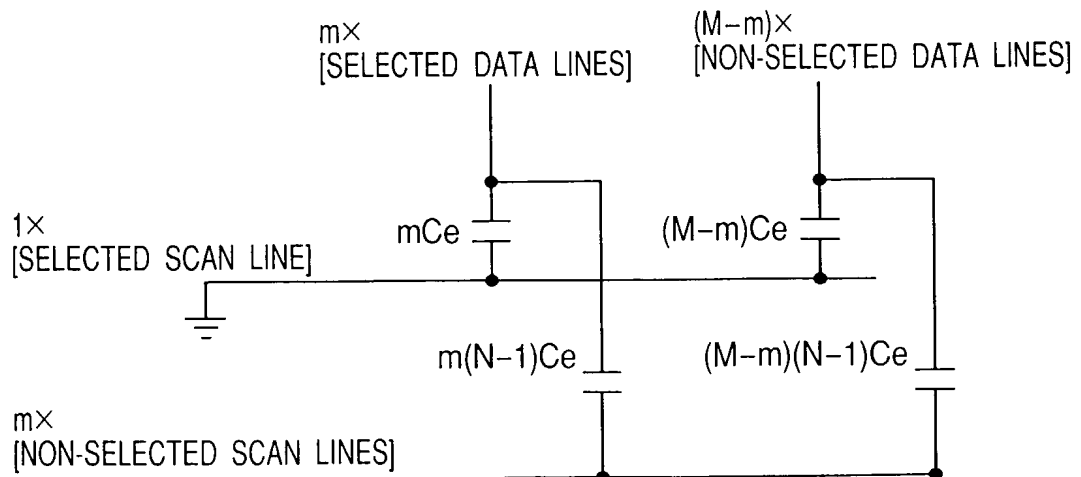


FIG. 5

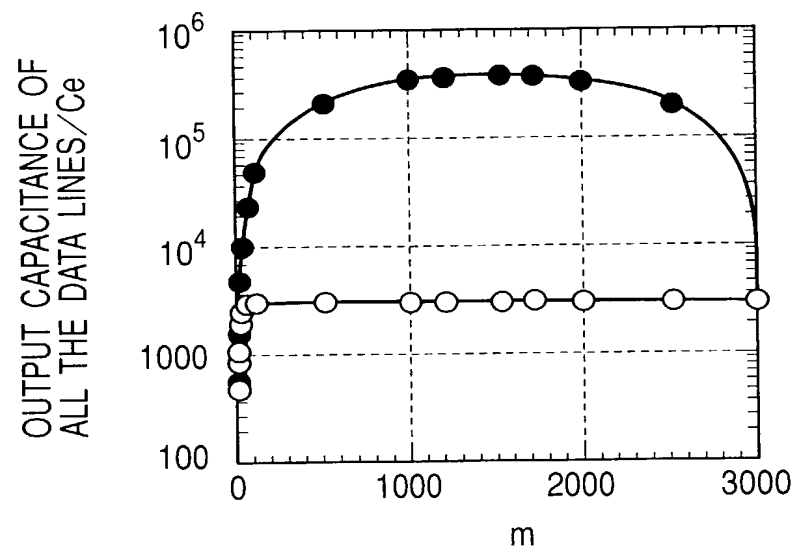


FIG. 6

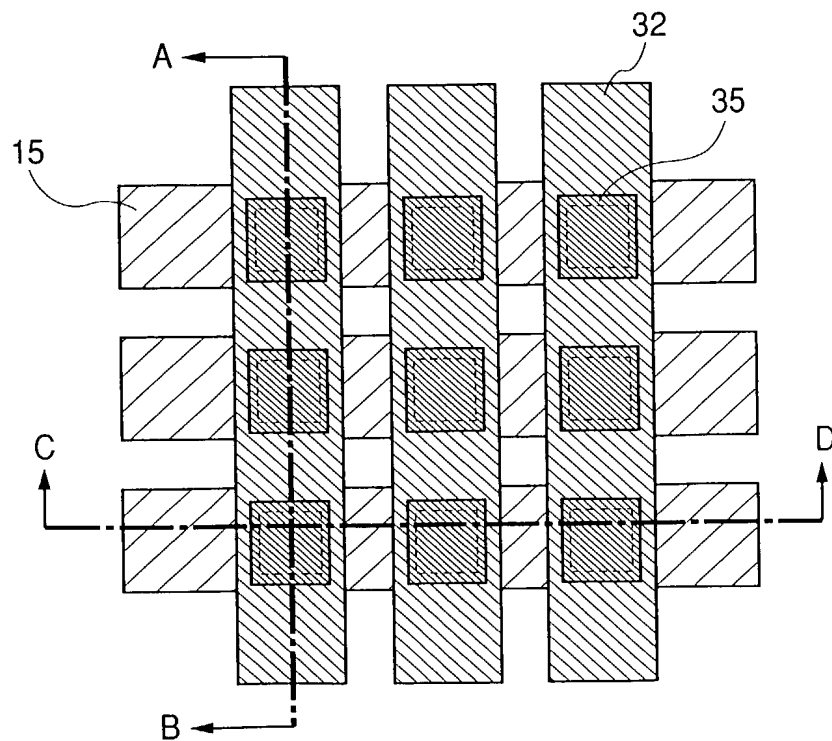


FIG. 7

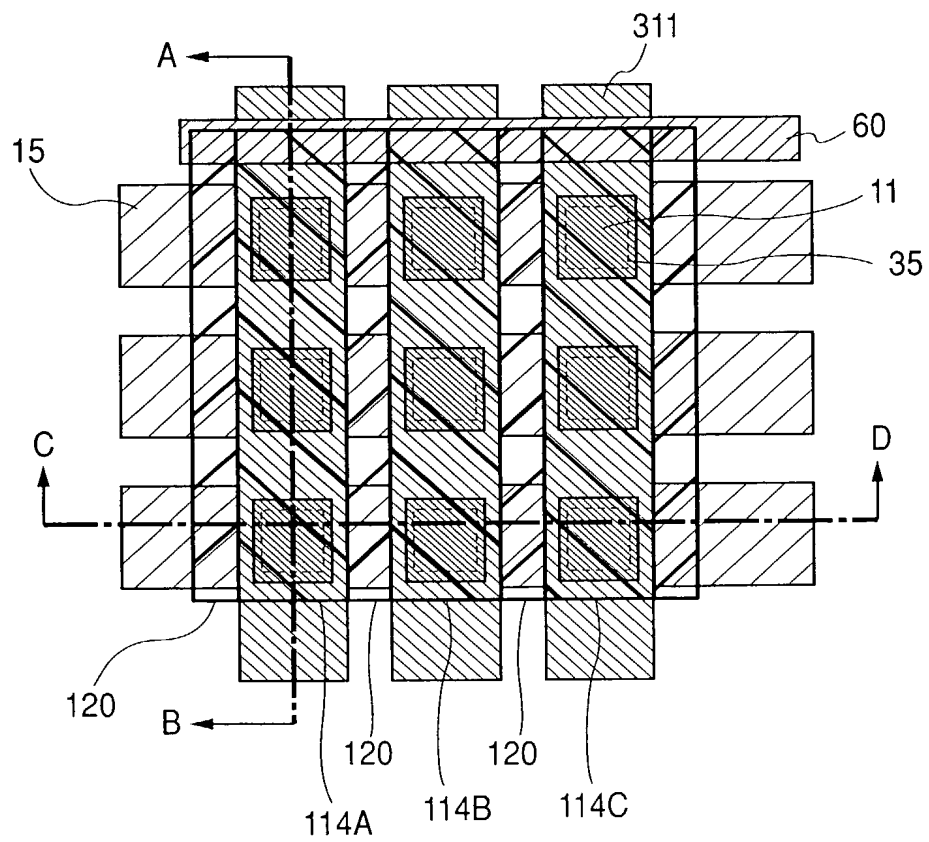
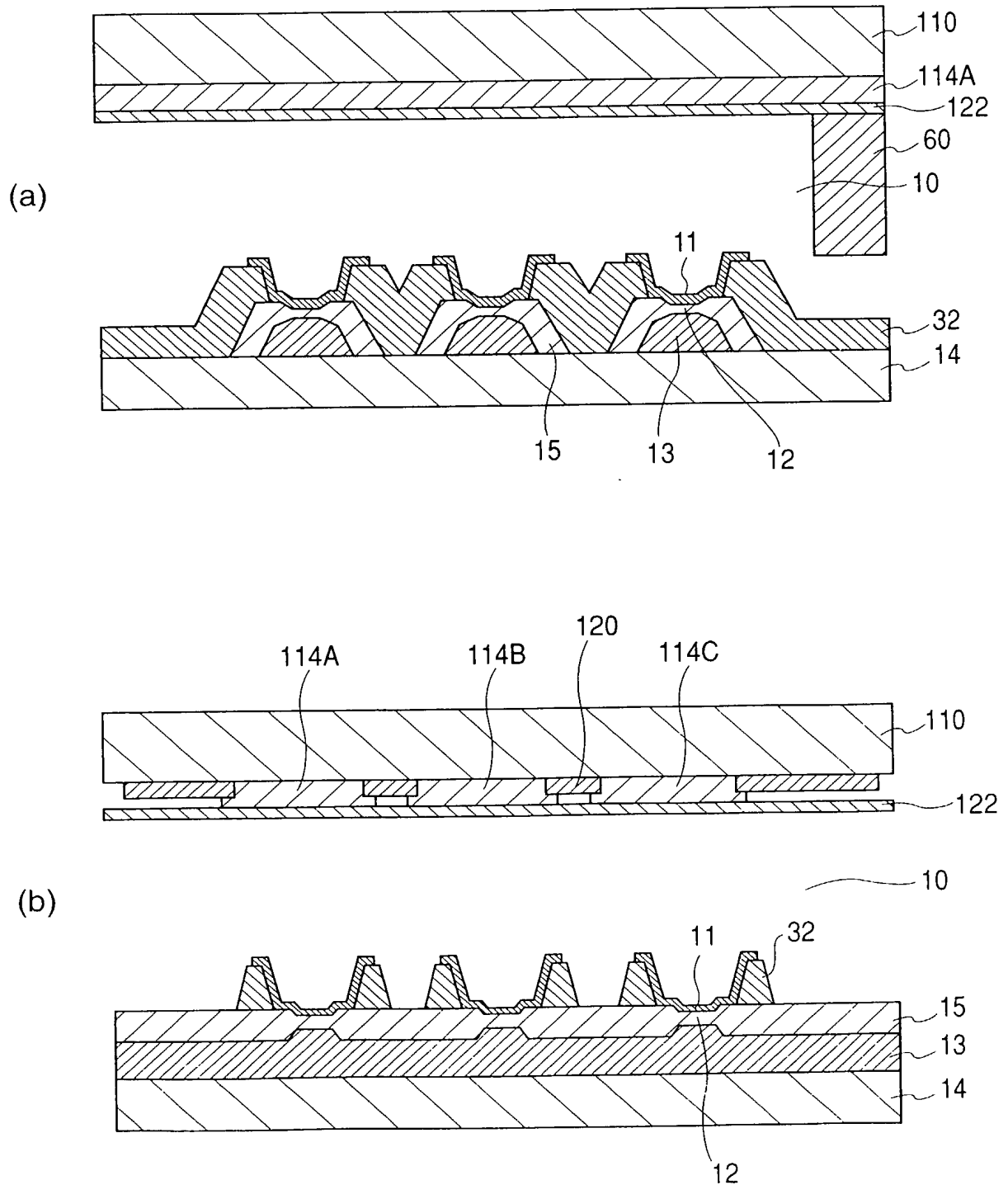


FIG. 8



6 / 9

FIG. 9

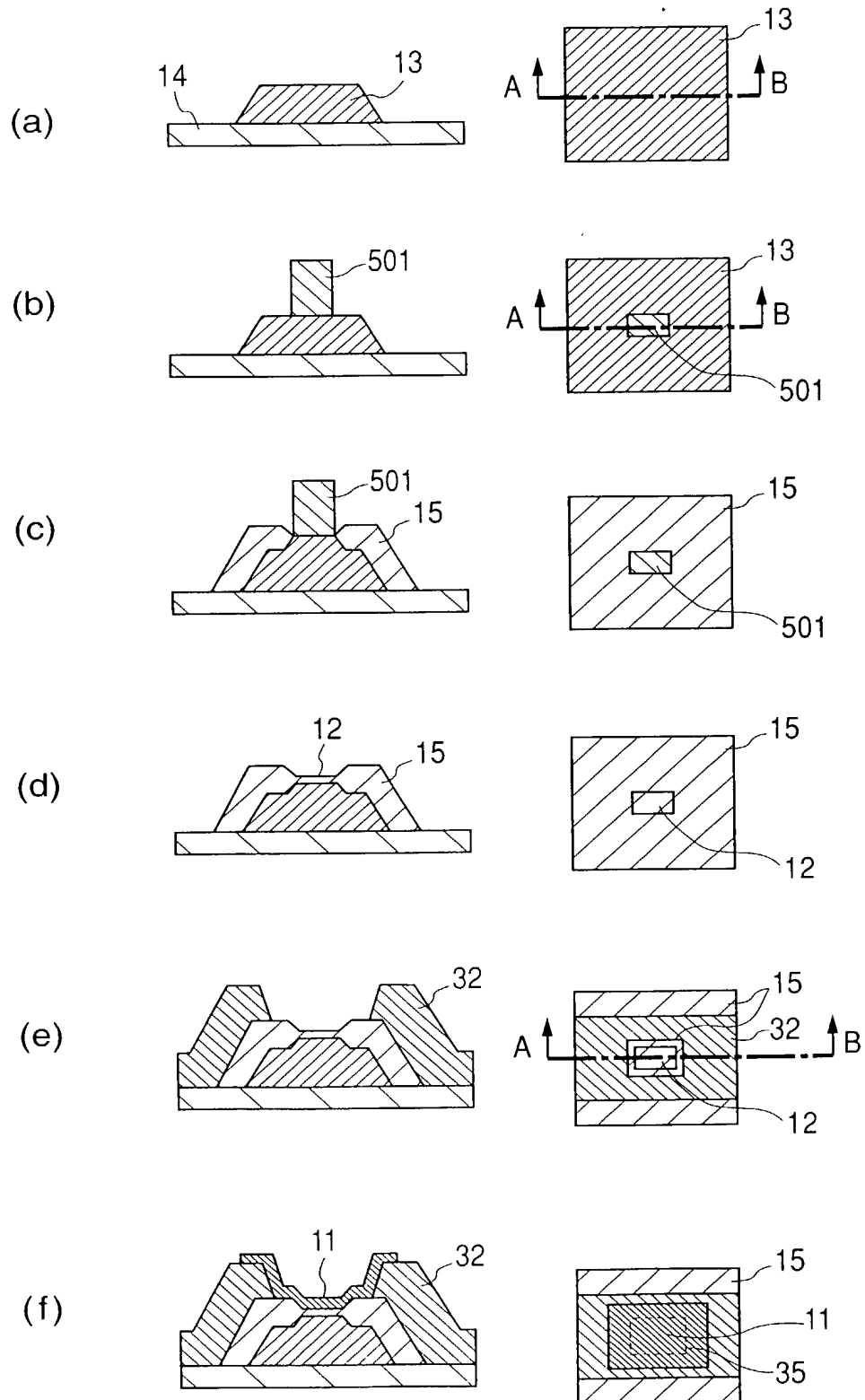


FIG. 10

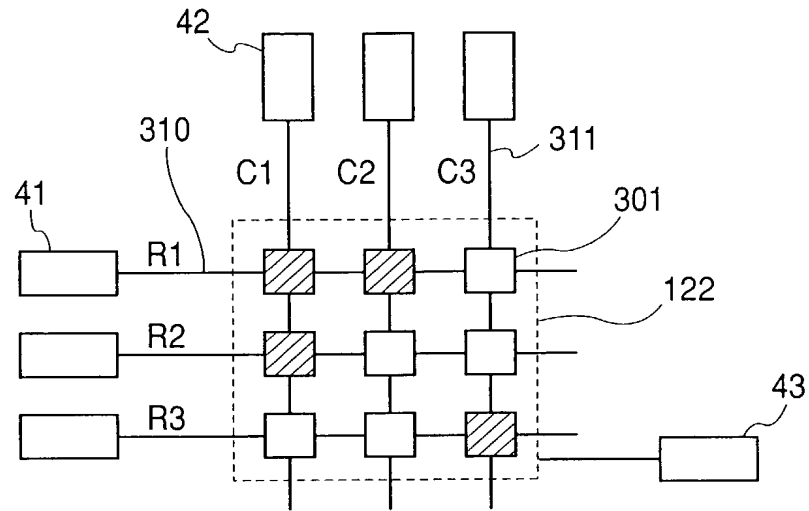


FIG. 11

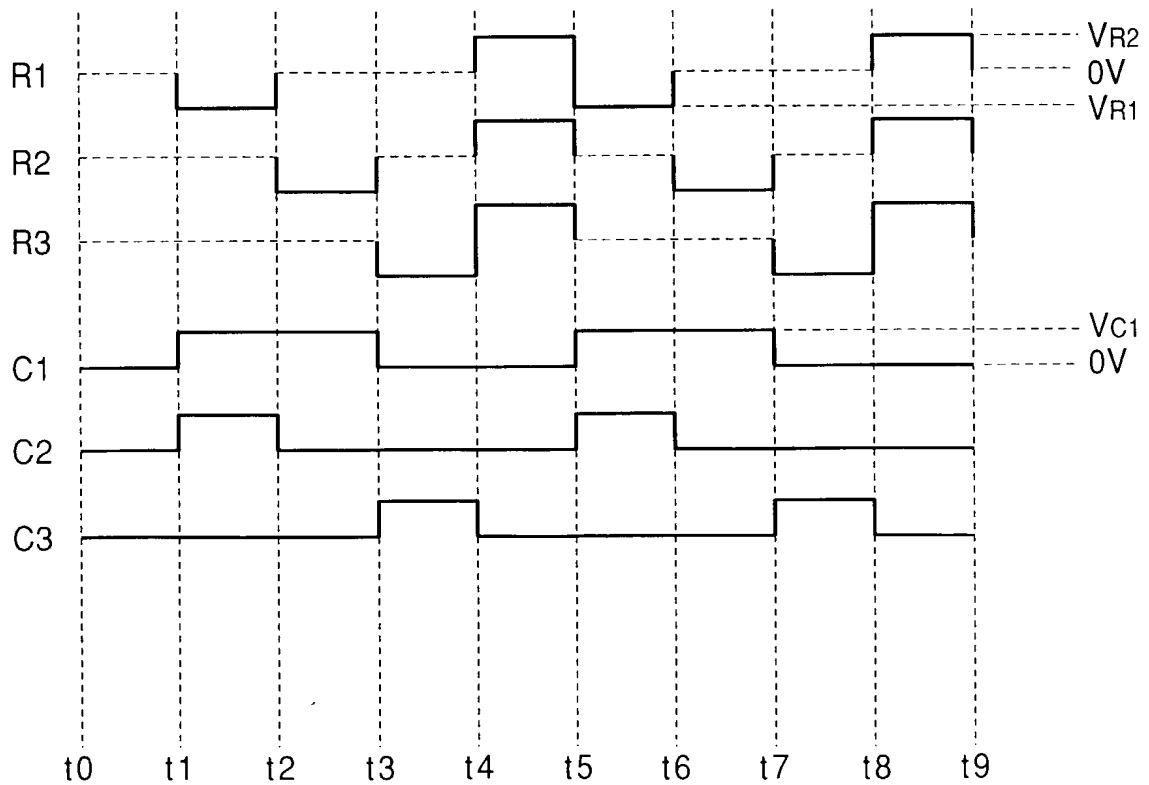


FIG. 12

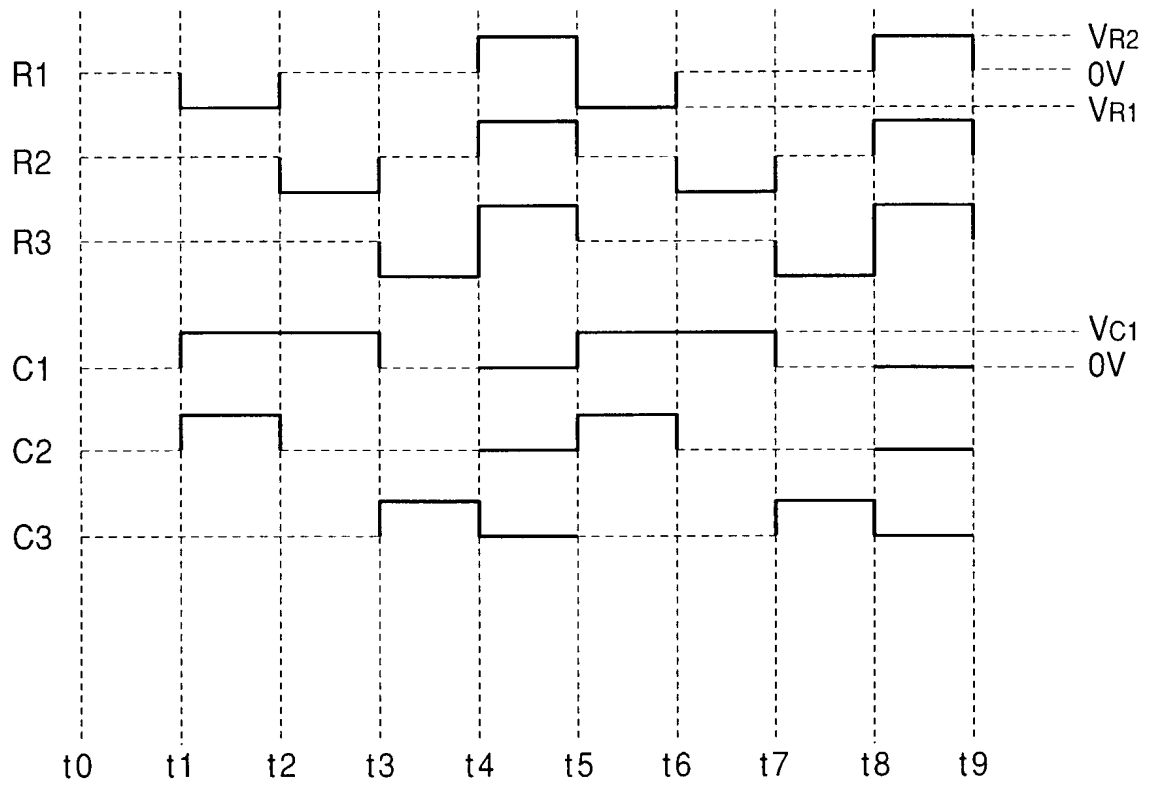


FIG. 13

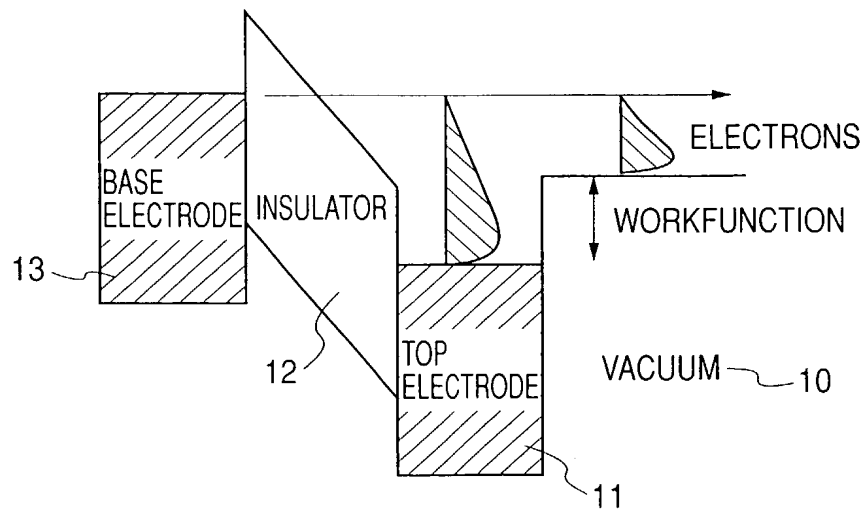


FIG. 14

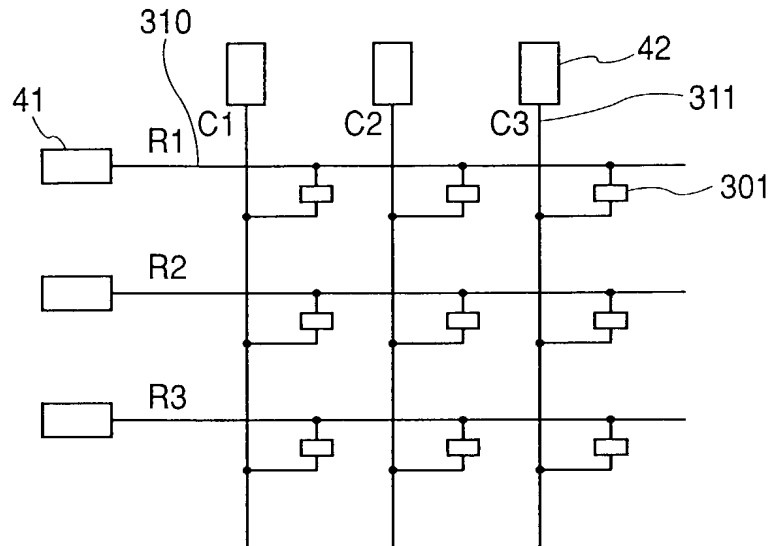
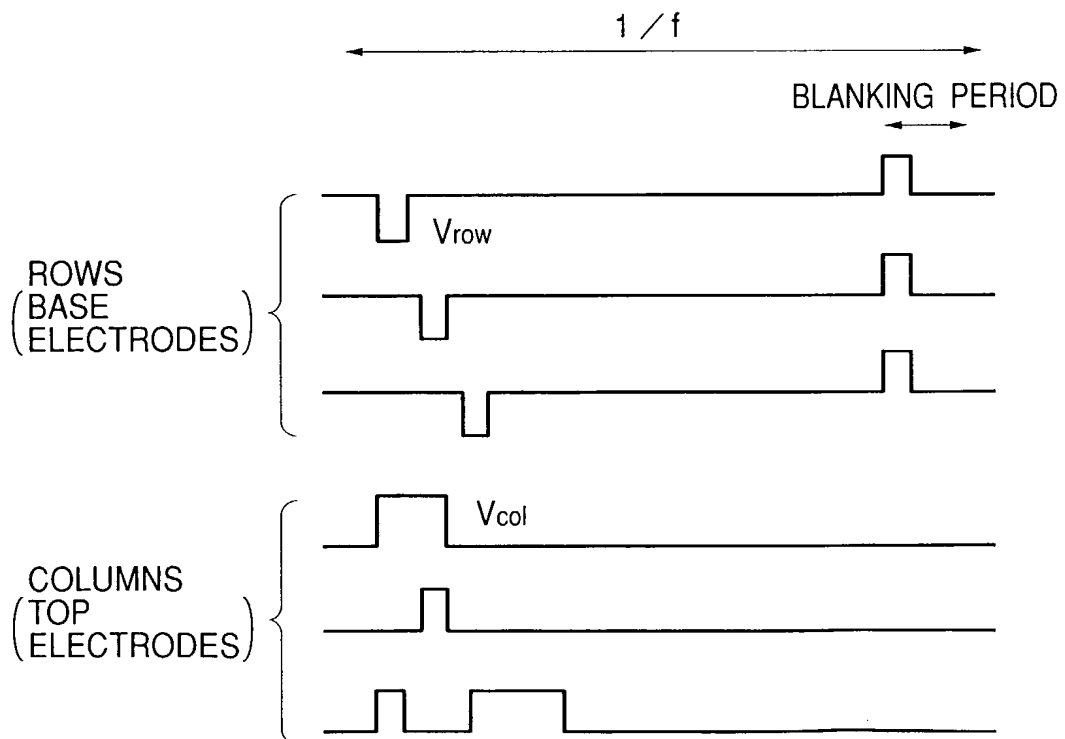


FIG. 15



Declaration and Power of Attorney For Patent Application

特許出願宣言書及び委任状

Japanese Language Declaration

日本語宣言書

下記の氏名の発明者として、私は以下の通り宣言します。

As a below named inventor, I hereby declare that:

私の住所、私書箱、国籍は下記の私の氏名の後に記載された通りです。

My residence, post office address and citizenship are as stated next to my name.

下記の名称の発明に関して請求範囲に記載され、特許出願している発明内容について、私が最初かつ唯一の発明者（下記の氏名が一つの場合）もしくは最初かつ共同発明者であると（下記の名称が複数の場合）信じています。

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

AN IMAGE DISPLAY AND A DRIVING

METHOD OF THE SAME

上記発明の明細書（下記の欄で×印がついていない場合は、本書に添付）は、

The specification of which is attached hereto unless the following box is checked:

☐ __月__日に提出され、米国出願番号または特許協定条約国際出願番号を____とし、
(該当する場合) _____に訂正されました。

☒ was filed on 4 / September / 2000 ✓
as United States Application Number or
PCT International Application Number
PCT/JP00/05989 ✓ and was amended on
20 / February / 2001 (if applicable).

私は、特許請求範囲を含む上記訂正後の明細書を検討し、内容を理解していることをここに表明します。

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

私は、連邦規則法典第37編第1条56項に定義されるとおり、特許資格の有無について重要な情報を開示する義務があることを認めます。

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number

Japanese Language Declaration (日本語宣言書)

私は、米国法典第35編119条(a)-(d)項又は365条(b)項に基づき下記の、米国外の国の少なくとも一カ国を指定している特許協力条約365(a)項に基づき国際出願、又は外国での特許出願もしくは発明者証の出願についての外国優先権をここに主張するとともに、優先権を主張している、本出願の前に出願された特許または発明者証の外国出願を以下に、枠内をマークすることで、示しています。

Prior Foreign Application(s)

外国での先行出願

11-256246 ✓ (Number) (番号)	Japan ✓ (Country) (国名)
 (Number) (番号)	 (Country) (国名)

I hereby claim foreign priority under Title 35, United States Code, Section 119 (a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Priority Not Claimed

優先権主張なし

9 / September / 1999 ✓ (Day/Month/Year Filed) (出願年月日)	<input type="checkbox"/>
 (Day/Month/Year Filed) (出願年月日)	<input type="checkbox"/>

私は、第35編米国法典119条(e)項に基づいて下記の米国特許出願規定に記載された権利をここに主張いたします。

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below.

(Application No.) (出願番号)	(Filing Date) (出願日)
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(Application No.) (出願番号)	(Filing Date) (出願日)
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私は、下記の米国法典第35編120条に基づいて下記の米国特許出願に記載された権利、又は米国を指定している特許協力条約365条(c)に基づき権利をここに主張します。また、本出願の各請求範囲の内容が米国法典第35編112条第1項又は特許協力条約で規定された方法で先行する米国特許出願に開示されていない限り、その先行米国出願書提出日以降で本出願書の日本国内または特許協力条約国際提出日までの期間中に入手された、連邦規則法典第37編1条56項で定義された特許資格の有無に関する重要な情報について開示義務があることを認識しています。

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s), or 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of Title 35, United States Code Section 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of application.

(Application No.) (出願番号)	(Filing Date) (出願日)
-----------------------------	------------------------

(Status: Patented, Pending, Abandoned) (現況: 特許許可済、係属中、放棄済)

(Application No.) (出願番号)	(Filing Date) (出願日)
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(Status: Patented, Pending, Abandoned) (現況: 特許許可済、係属中、放棄済)

私は、私自身の知識に基づいて本宣言書中で私が行なう表明が真実であり、かつ私の入手した情報と私の信じることに基づき表明が全て真実であると信じていること、さらに故意になされた虚偽の表明及びそれと同等の行為は米国法典第18編第1001条に基づき、罰金または拘禁、もしくはその両方により処罰されること、そしてそのような故意による虚偽の声明を行えば、出願した、又は既に許可された特許の有効性が失われることを認識し、よってここに上記のごとく宣誓を致します。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Japanese Language Declaration (日本語宣言書)

委任状： 私は下記の発明者として、本出願に関する一切の手続きを米特許商標局に対して遂行する弁理士または代理人として、下記の者を指名いたします。(弁護士、または代理人の氏名及び登録番号を明記のこと)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith (list name and registration number)

2 -

Stanley P. Fisher, Reg. No. 24,344 and Juan Carlos Marquez,
Reg. No. 34,072

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唯一または第一発明者名

Full name of sole or first inventor

Mutsumi SUZUKI

発明者の署名 日付

Inventor's signature Date

Mutsumi Suzuki 1/15/2002

住所

Residence

Kodaira, Japan JPX

国籍

Citizenship

Japan ✓

私書箱

Post Office Address

c/o Hitachi, Ltd., Intellectual Property Group
New Marunouchi Bldg. 5-1, Marunouchi 1-chome,
Chiyoda-ku, Tokyo 100-8220, Japan

(第二以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for second and subsequent joint inventors.)

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2-00	第二共同発明者名	Full name of second joint inventor, if any <u>Toshiaki KUSUNOKI</u>
	第二共同発明者の署名 日付	Second inventor's signature Date <u>Toshiaki Kusunoki</u> 1/15/2002
	住所	Residence <u>Tokorozawa, Japan JPX</u>
	国籍	Citizenship <u>Japan</u> ✓
	私書箱	Post Office Address c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan
3-00	第三共同発明者名	Full name of third joint inventor, if any <u>Makoto OKAI</u>
	第三共同発明者の署名 日付	Third inventor's signature Date <u>Makoto Okai</u> 1/16/2002
	住所	Residence <u>Tokorozawa, Japan JPX</u>
	国籍	Citizenship <u>Japan</u> ✓
	私書箱	Post Office Address c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan
4-00	第四共同発明者名	Full name of fourth joint inventor, if any <u>Masakazu SAGAWA</u>
	第四共同発明者の署名 日付	Fourth inventor's signature Date <u>Masakazu Sagawa</u> 1/16/2002
	住所	Residence <u>Inagi, Japan JPX</u>
	国籍	Citizenship <u>Japan</u> ✓
	私書箱	Post Office Address c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan
5-00	第五共同発明者名	Full name of fifth joint inventor, if any <u>Akitoshi ISHIZAKA</u>
	第五共同発明者の署名 日付	Fifth inventor's signature Date <u>Akitoshi Ishizaka</u> 1/21/2002
	住所	Residence <u>Chiba, Japan JPX</u>
	国籍	Citizenship <u>Japan</u> ✓
	私書箱	Post Office Address c/o Hitachi, Ltd., Intellectual Property Group New Marunouchi Bldg. 5-1, Marunouchi 1-chome, Chiyoda-ku, Tokyo 100-8220, Japan

(第六以降の共同発明者についても同様に記載し、署名をすること)

(Supply similar information and signature for sixth and subsequent joint inventors.)